Look-up Table Index Value Generation in a Turbo Decoder

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ABSTRACT OF THE DISCLOSURE

An index value generation circuit for use in a turbo decoder for computing the index value $z = |x_1 - x_2|$ for addressing a table used for computing the function $\log(e^{x_1} + e^{x_2})$ or $\ln(e^{x_1} + e^{x_2})$ is described. Parameters x_1 and x_2 are first and second argument values derived from the input data. The index value generation circuit computes the difference of the first argument x_1 and the second argument value x_2 by taking the 2's compliment of the second argument value and adding the first argument value to the negative value of the second argument value x_2. If the difference is a negative number, the index value generation circuit computes the absolute value of the difference by taking the 1's compliment of the difference $x_1 - x_2$. In this manner, the index value z used to address the table for computing the function $\log(e^{x_1} + e^{x_2})$ or $\ln(e^{x_1} + e^{x_2})$ in the decoding operation can be generated quickly. Furthermore, the index value generation circuit of the present invention simplifies the computation process and enhances the performance of the turbo decoder.